CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a plurality of memory blocks each having a plurality of static memory cells, a first local bit line connected to said static memory cells, and a first amplifier for amplifying voltage of said first local bit line;

a first global bit line connected to an output of said first amplifier to transfer read data amplified by said first amplifier of each of said memory blocks; and

precharging circuits connected to both ends of said first global bit line, respectively, to precharge said first global bit line to a first power supply voltage.

2. The semiconductor memory according to claim 1, wherein

said first power supply voltage is an external power supply voltage supplied from the exterior of the semiconductor memory.

3. The semiconductor memory according to claim 1, wherein

said precharging circuits each have a first transistor whose gate receives a control signal being activated in a precharge operation, whose drain is connected to said first global bit line, and whose source is connected to a first power supply line for supplying said first power supply voltage.

4. The semiconductor memory according to claim 3, wherein:

said first amplifier has a second transistor whose gate receives the voltage of said first local bit line, whose drain is connected to said first global bit line, and whose source is connected to a second power supply line for supplying a second power supply voltage; and

said first transistor of each of said precharging circuits and said second transistor of said first amplifier are inverse in polarity.

5. The semiconductor memory according to claim 1, wherein

said first amplifier has a second transistor whose gate receives the voltage of said first local bit line, whose drain is connected to said first global bit line, and whose source is connected to a second power supply line for supplying a second power supply voltage.

6. The semiconductor memory according to claim 1, wherein

said memory blocks each have a second local bit line connected to said static memory cells to transfer data complementary to the data transferred to said first local bit line.

7. The semiconductor memory according to claim 1, wherein

said first global bit line is laid along the direction in which said memory blocks are arranged.

8. The semiconductor memory according to claim 1, further comprising

a second global bit line for transferring write data to said static memory cells, and wherein

said memory blocks each have a second amplifier for amplifying voltage of said second global bit line and outputting the amplified data to said first local bit line.

9. The semiconductor memory according to claim 1, wherein

said first global bit line is laid in parallel with said first local bit line.